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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,603	08/30/2001	Gary L. Swoboda	TI-30491	2424

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,603	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *August 28, 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on August 30, 2001.

2. Claims 1- 20 have been examined and rejected.

Priority

3. The priority date considered for this application is March 02, 2000.

Information Disclosure Statement

4. The Office acknowledges receipt of the Information Disclosure Statement filed on August 28, 2002. It has been placed in the application file and the information referred to therein has been considered.

Oath/Declaration

5. The Office acknowledges receipt of a properly signed oath/declaration filed on August 30, 2001.

Specification

6. The disclosure is objected to because of the following informalities: The specification does not include a Brief Summary of the Invention.

Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

Appropriate correction is required.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-20 are rejected under the judicially created doctrine of double patenting over claims 1-30 of U. S. Patent No. 6,912,675 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

As per Issued Claim 1 and Instant Claim 1:

Issued Claim 1	Instant Claim 1
A method of exporting from a data processor a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by the data processor, comprising:	A method of exporting from a data processor an emulation parameter value indicative of a data processing operation performed by the data processor, comprising:
	providing the parameter value as a plurality of digital bits;
detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value; and	detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of the first group; and
in response to detection of said condition, outputting, via terminals of the data processor, said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value	in response to detection of said condition, outputting from the data processor via terminals thereof only the second group of bits without outputting the first group of bits

As can be seen from the table, the only difference between the Issued Claim and instant claim is that the instant Claim has an extra limitation (i.e. the parameter value as a plurality of digital bits). It would have been obvious to one of ordinary skill in the art to define the parameter value as a plurality of digital bits. This would help to be more specific what the parameter value stands for.

As per Issued Claim 17 and Instant Claim 11:

Issued Claim 17	Instant Claim 11
An integrated circuit, comprising:	An integrated circuit, comprising:
a data processor for performing data processing operations;	a data processor for performing data processing operations
a plurality of terminals for outputting information;	a plurality of terminals for outputting information;
an apparatus for exporting from said integrated circuit a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving	an apparatus for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits; said apparatus including an

said parameter values, and an information generator coupled to said input for detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value, said information generator operable for providing information which indicates that said condition has been detected;	evaluator coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group, said evaluator operable for providing condition information which indicates that said condition has been detected;
and said apparatus further including a compression determiner coupled to said information generator and said input and said terminals, said compression determiner responsive to said condition information for outputting via said terminals said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value	and said apparatus including a compression determiner coupled to said evaluator and said terminals and said input, said compression determine responsive to said condition information for outputting via said terminals only the second group of bits without outputting the first group of bits.

The only difference between Issued Claim 17 and Instant Claim 11 is: Issued claim17 has a limitation of information generator and Instant claim 11 has a limitation of an evaluator. However, both these limitations have the same purpose for detecting a condition of the same bit values. It would have been obvious to one of ordinary skill in the art to inter exchange between the information generator and an evaluator because of their similarity on their usage in the invention.

As per Issued Claim 28 and Instant Claim 18:

Issued Claim 28	Instant Claim 18
A data processing system, comprising:	A data processing system, comprising:
an integrated circuit, including a data processor for performing data processing operations;	an integrated circuit, including a data processor for performing data processing operations;
an emulation controller coupled to said integrated circuit for controlling emulation operation of said data processor;	an emulation controller coupled to said integrated circuit for controlling emulation operation of said data processor;
said integrated circuit including an apparatus coupled between said data processor and said emulation controller for exporting from said integrated circuit a plurality of parameter values of an emulation parameter that is indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter values, and an information generator coupled to said input for	said integrated circuit including an apparatus coupled between said data processor and said emulation controller for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits; said apparatus including an evaluator coupled to said input for detecting a condition wherein the bits of a first group within the plurality of

detecting a condition wherein a first portion of a first said parameter value is identical to a corresponding portion of a second said parameter value, said information generator operable for providing information which indicates that said condition has been detected; and	bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group, said emulator operable for providing condition information which indicates that said condition has been detected; and
said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, and said apparatus further including a compression determiner coupled to said information generator and said input and said terminals, said compression determiner responsive to said condition information for outputting to said emulation controller, via said terminals, said second parameter value and only a remainder portion of said first parameter value other than said first portion of said first parameter value	said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, and said apparatus including a compression determiner coupled to said evaluator and said terminals and said input, said compression determiner responsive to said condition information for outputting to said emulation controller, via said terminals, only the second group of bits without outputting the first group of bits.

Instant claim 18 has one extra limitation of an evaluator, which has the same purpose as information generator, which is included in Issued claim 28. Therefore, it would have been obvious to one of ordinary skill in the art to inter exchange between the information generator and an evaluator because of their similarity on their usage in the invention.

The same rationale is also applicable for the rejection of the Instant Claims 6, 7, 8, 15, 19, and 20 based on an Issued Claims 10, 11, 12, 27, 29, and 30.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

10. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application No. 6, 779, 145 issued to Edwards.

As per Claim 1:

Edwards teaches providing the parameter value as a plurality of digital bits (col. 5 line 40); detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of the first group (Col. 12 lines 4-16); and in response to detection of said condition, outputting from the data processor via terminals thereof only the second group of bits without outputting the first group of bits (col. 12 lines 17-26).

As per Claim 2:

Edwards teaches receiving only the second group of bits externally of the data processor (Fig. 5 element 509), and recreating the first group of bits based on the bit value of said predetermined bit (Fig. 5 element 501).

As per Claim 3:

Edwards discloses at least one byte, the second group of bits includes at least one byte, and the predetermined bit is a most significant bit of said at least one byte of the second group (col. 24 lines 58-60).

As per Claim 4:

Edwards discloses a plurality of bytes and the predetermined bit is a most significant bit of one of the bytes of the second group (col. 24 lines 58-60).

As per Claim 5:

Edwards discloses one byte of the second group is a most significant byte of the second group (col. 24 lines 58-60).

As per Claim 6:

Edwards discloses a program counter value (col. 9 line 51).

As per Claim 7:

Edwards discloses a memory address value (value which is stored at a memory address; col. 10 line 48).

As per Claim 8:

Edwards discloses a memory data value (col. 12 lines 12-13).

As per Claim 9:

Edwards discloses a bit value of said predetermined bit and said bits of said first group is a 1. (*If the value of PC Absolute is `1`, this field holds a 4-byte absolute value of the program counter*; table 1 col. 13).

As per Claim 10:

Edwards discloses bit value of said predetermined bit and said bits of said first group is 0 (*If the value of PC Absolute is `0`, this field is a 4-bytes 1-byte or 2-byte compressed address as a signed offset from the most recent program counter value sent in a previous trace message;* table 1 col. 13).

As per Claim 11:

Edwards discloses integrated circuit (integrated circuit 101; Fig. 1):

a data processor (Col. 6 lines 54-56; Fig. 1 element 102) for performing data processing operations;

a plurality of terminals (Fig. 6 elements 602-610) for outputting information;

an apparatus for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits (col. 8 lines 43-44; Fig. 2 elements 208A and 208B);

an evaluator (watch point channel; col. 12 lines 5-12) coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits all have

the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group, said evaluator operable for providing condition information which indicates that said condition has been detected;

a compression determiner (col. 3 lines 20-21) coupled to said evaluator and said terminals and said input, said compression determiner responsive to said condition information for outputting via said terminals only the second group of bits without outputting the first group of bits.

As per Claim 12:

The limitation of claim 12 has already been discussed in the rejection of claim 3. It is therefore rejected under the same rationale.

As per Claim 13:

The limitation of claim 13 has already been discussed in the rejection of claim 4. It is therefore rejected under the same rationale.

As per Claim 14:

The limitation of claim 14 has already been discussed in the rejection of claim 5. It is therefore rejected under the same rationale.

As per Claim 15:

The limitation of claim 15 has already been discussed in the rejection of claims 6, 7, and 8. It is therefore rejected under the same rationale.

As per Claim 16:

The limitation of claim 16 has already been discussed in the rejection of claim 9. It is therefore rejected under the same rationale.

As per Claim 17:

The limitation of claim 17 has already been discussed in the rejection of claim 10. It is therefore rejected under the same rationale.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

12. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 6, 779, 145 issued to Edwards as applied to claims 1-17 above, and further in view of U.S. Patent Application No. 5, 572, 710 issued to Asano.

As per Claim 18:

Edwards discloses:

a data processor (Col. 6 lines 54-56; Fig. 1 element 102) for performing data processing operations;

a compression determiner (col. 3 lines 20-21) coupled to said evaluator and said terminals and said input, said compression determiner responsive to said condition information for outputting to said emulation controller, via said terminals, only the second group of bits without outputting the first group of bits.

an evaluator (watch point channel; col. 12 lines 5-12) coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group

Edwards fails to disclose:

an emulation controller coupled to said integrated circuit for controlling emulation operation of said data processor,

emulator operable for providing condition information which indicates that said condition has been detected;

a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller,

an apparatus coupled between said data processor and said emulation controller for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits

Asano discloses:

an emulation controller (Fig. 2 element 8) coupled to said integrated circuit for controlling emulation operation of said data processor;

emulator (Fig. 10 element 4) operable for providing condition information which indicates that said condition has been detected;

a plurality of terminals (Fig. 2 element 2) coupled to said emulation controller for outputting information to said emulation controller, an apparatus (Fig. 2 element 2) coupled between said data processor and said emulation controller for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Edwards related to flow control between integrated circuit and external system for debugging information and system bus transaction

information with the teachings of Asano related to a logic simulation system handling a very large scale circuit by interconnecting the plurality of emulation chips. The motivation for doing so would have been more convenient to add the debugging ability in the system by adding the emulator and emulator controller. Hence a skilled artisan having access to the teaching of Edwards and Asano would have knowingly modified the teaching of Edwards with Asano.

As per Claim 19:

Asano discloses a man/machine interface coupled to emulation controller for permitting a user to communicate with emulation controller (Fig. 2 element 8).

As per Claim 20:

Edwards discloses one of a visual interface and a tactile interface (First and second interfaces; col. 5 lines 20-23).

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Jean R. Homere can be reached at (571) 272-3780. The official fax number is (703) 872-9306. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

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